REMARKS

Claims 1-9, 12-14, 29, and 31-38, are all the claims pending in the application. Claims 10-11, 15-28, and 30 are cancelled; and, claims 1-14, 29, and 31-38 stand rejected on prior art grounds. Applicants respectfully traverse the rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 5-6, 8, 12-13, 29, 32, 34-35, and 37-38 stand rejected under 35 U.S.C. §102(e) as being anticipated by She, et al. (U.S. Publication No. 2005/0242391), hereinafter referred to as She. Claims 1, 3-4, 7-8, 10-11, 14, 29, and 34 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hsu, et al. (U.S. Patent No. 6,107,141), hereinafter referred to as Hsu. Claims 2, 9, 31, and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over She. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a multiple-gate transistor comprising a logic gate, a floating gate, and a programming gate, which the Office Action argues is disclosed in She. However, the structure of She only has two gates, wherein the "trapping layer" of She is an insulator and therefore does not disclose a gate structure. Moreover, the Bit 1 and Bit 2 of the trapping layer do not disclose a gate; instead, the Bit 1 and Bit 2 "are source storage bit and drain storage bit (two bits/gate) associated with each gate" (i.e., the Control Gate 2). Nothing within the cited prior art teaches that the Bit 1 and Bit 2 of the trapping layer affects the channel region. As such, the trapping layer does not teach a

gate structure. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

A. The Rejections Based on She

The Office Action argues that She discloses a floating gate (Office Action, p. 5, item no. 4). More specifically, referencing figures 10 and 11 of She, the Office Action argues that a trapping layer (where Bit 1 and Bit 2 are trapped) is analogous to the floating gate of the claimed invention. Applicants respectfully disagree with such a conclusion. Specifically, the alleged trapping layer of She is not a transistor gate structure because gates are conductors.

First of all, even if the Office Action is correct that the silicon nitride (see FIGS. 1, 2E, and 2G) might hold charges does not mean that it is any form of gate. Just because a layer holds charge does not necessarily make it a gate. As is commonly known within the art, a gate is a conductor. Nitrides are insulators.

Furthermore, figures 10 and 11 and the accompanying text only disclose two (2) control gates: control gate 1 (which the Office Action asserts teaches the logic gate of the claimed invention); and, control gate 2 (which the Office Action asserts teaches the programming gate of the claimed invention). However, these gates perform the same function and are the same type of gate (i.e., control gates). More specifically, paragraph 0035 of She provides that "[t]here are source storage bit and drain storage bit (*two bits/gate*) associated with each gate, hence a *total* of 4 physical bit/cell is realized with the above structure."

Since there are only four 4 "total" bits shown, and two bits are provided per control gate, only two control gates are disclosed figures 10 and 11 (i.e., gate 1 and gate 2). If the trapping layer were a gate, there would be three total gates and six total bits; however, the drawings do not illustrate such a structure. Figures 10 and 11 and the accompanying text clearly show that the structure only has four total bits (See paragraph 0035 of She, "hence a total of 4 physical bit/cell is realized with the above structure").

Accordingly, Applicants submit that She fails to teach a logic gate, a programming gate, and a floating gate. Instead, She discloses a structure having only two gates. The alleged "trapping layer" of She is an insulator and therefore does not disclose a gate structure. As such, it is Applicants' position that She fails to the claimed feature of "A multiple-gate transistor comprising … a floating gate" as defined by independent claims 1, 8, 29, and 35.

The Office Action also argues that She discloses a floating gate that adjusts the threshold voltage of the transistors because "this is inherent characteristics of floating gate transistor" (Office Action, p. 9, para. 1). Such features are defined in independent claims 29 and 34, and in dependent claims 4 and 11, using similar language.

As discussed more fully above, the alleged trapping layer of She does not teach a floating gate. Therefore, contrary to the position taken in the Office Action, She does not inherently teach a floating gate that adjusts the threshold voltage of the transistors.

In addition, the Office Action argues that She discloses a logic gate (Office Action, p. 5, item 4, citing figures 10-11 of She). Applicants respectfully disagree with

such a conclusion. Instead, She discloses a structure having two control gates and zero logic gates.

Specifically, as provided in paragraph 0032 of She, a 4 physical bit/cell can be realized by breaking the top portion of the control gate on top of each channel. For example, a folded control gate in FIG. 6A is broken into *two control gates* by using a chemical mechanical polishing (CMP) method. As shown in FIG. 8, these *two control gates* control each vertical side of the channel region. Here the front gate is called "gate1" and the back gate is called "gate 2" in each memory cell.

The Office Action asserts that the gate 1 of She is a logic gate (Office Action, p. 5, item 4). However, as discussed above, the gate 1 is a control gate, not a logic gate. Therefore, Applicants submit that, contrary to the position taken in the Office Action, She fails to teach the claimed feature of a logic gate, as defined by independent claims 1, 8, 29, and 35, "wherein voltage in said logic gate causes said transistor to switch on and off" as defined by independent claims 29 and 35.

Moreover, even if the Office Action is correct in that the gate 1 is a logic gate and that the gate 2 is a programming gate, the gate 1 and the gate 2 each perform the same function, i.e., they are both "control gates" (She, para. 0032). Therefore, She fails to teach the claimed feature "wherein said logic gate performs a different function than said floating gate, wherein said logic gate performs a different function than said programming gate, and wherein said floating gate performs a different function than said programming gate" as defined by independent claims 1 and 8. Additionally, She fails to teach the claimed feature "wherein voltage in said logic gate causes said transistor to

switch on and off … and wherein charge in said floating gate adjusts the threshold voltage of said transistor" as defined by independent claims 29 and 35.

In regards to whether the trapping layer of She teaches a transistor gate structure, and more specifically whether the trapping layer affects the channel of the transistor, the Office Action argues that:

> [i]t is well known in the art that when charges are trapped in a trapping layer formed between a channel and a control gate (Gate 2), as that taught by She, such charges would electrically affect the conductivity of the channel due to electrical field caused by the charges. Hence, technically, the charges trapped in the trapping layer, or the trapping layer, does affect the channel region

(Office Action, p. 2, item 2). However, the Office Action fails to provide any support to maintain its assertion that charges within the trapping layer create an electrical field that electrically affects the conductivity of the channel.

Applicants submit that nothing within the cited prior art teaches that the trapping layer of She affects the channel. Accordingly, it is Applicants' position that the trapping layer does not disclose a transistor gate structure. Therefore, contrary to the position taken in the Office Action, the trapping layer does not teach the floating gate of the claimed invention.

Applicants further traverse the rejections because, contrary to the position taken in the Office Action, She does not disclose the claimed feature "wherein said logic gate performs a different function than said floating gate, wherein said logic gate performs a

different function than said programming gate, and wherein said floating gate performs a different function than said programming gate". Such features are defined in independent claims 1 and 8.

The Office Action argues that the trapping layer of She can perform a different function than the Gate 1 (which the Office Action argues teaches the logic gate of the claimed invention) and the Gate 2 (which the Office Action argues teaches the programming gate of the claimed invention) (Office Action, p. 3, para. 2). However, as more fully described above, the trapping layer does not disclose a gate; and therefore cannot disclose a logic gate.

The Office Action also argues that the Gate 1 can perform a different function than the Gate 2 because the Gate 1 is capable of storing Bit 3 and Bit 4 while the Gate 2 is not (Office Action, p. 3, para. 2). The Office Action fails to provide any support to maintain this assertion. Using the Office Action's logic that Gate 1 is capable of storing Bit 3 and Bit 4, then the Gate 2 should be capable of storing Bit 1 and Bit 2 (Gate 2 performs the same function as Gate 1). Furthermore, as described in paragraph 0035 of She, "[t]here are source storage bit and drain storage bit (two bits/gate) associated with each gate". Therefore, Bit 3 and Bit 4 are associated with Gate 1; and, Bit 1 and Bit 2 are associated with Gate 2.

Further contrary to the position taken in the Office Action, the Bit 1 and Bit 2 is NOT a gate. Instead, the Bit 1 and Bit 2 "are source storage bit and drain storage bit (two bits/gate) associated with each gate" (i.e., the Gate 2). The Office Action asserts that the Bit 1 and Bit 2 disclose a gate structure; however, such an assertion would be inconsistent

with the teachings of She because there is no source storage bit and drain storage bit associated with the Bit 1 and Bit 2 – as discussed above, "[t]here are source storage bit and drain storage bit (two bits/gate) associated with each gate" (She, para. 0035).

B. The Rejection Based on Hsu

Applicants traverse this rejection because Hsu teaches that the channel region is entirely below the select gate (which the Office Action asserts teaches the logic gate of the claimed invention) and the floating gate, whereas the claimed invention defines that "said channel region is between said floating gate and said logic gate" (independent claims 1, 8, 29, and 35).

More specifically, the Office Action asserts that the top surface of the substrate 10, between the drain region 20 and the source region 30, teaches the channel region of the claimed invention (Office Action, p. 12, para. 3). As illustrated in FIG. 1 of Hsu, the asserted channel region is entirely below the select gate 120 (which the Office Action asserts teaches the logic gate of the claimed invention (Office Action, p. 12, para. 3)) and the floating gate 130. The asserted channel region is NOT between the select gate 120 and the floating gate 130.

To the contrary, as illustrated in FIG. 15 of Applicants' disclosure, the silicon fin 142 is between the logic gate 130 and the floating gate 30. Further, as described in paragraph 0029 of Applicants' disclosure, "the silicon fin 142 comprises a channel region". Thus, because the silicon fin 142 comprises a channel region, and because the

silicon fin 142 is between the logic gate 130 and the floating gate 30, the transistor includes a channel region that is between the logic gate 130 and the floating gate 30.

Accordingly, Applicants submit that unlike the claimed invention, Hsu does not teach a channel region between a floating gate and a logic gate. Instead, the channel region of Hsu is entirely below (and therefore cannot be between) the floating gate and the asserted logic gate. Therefore, it is Applicants' position that Hsu fails to teach the claimed feature "wherein said channel region is between said floating gate and said logic gate" as defined by independent claims 1, 8, 29, and 35.

Therefore, it is Applicants' position that She and Hsu do not teach or suggest many features defined by independent claims 1, 8, 29, and 35 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9, 12-14, 31-34, and 36-38 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-9, 12-14, 29, and 31-38, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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